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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,122	01/13/2004	Wai-Fan Yau	AMAT/2592.C7/DSM/LOW K/JW	4554

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PATTERSON & SHERIDAN, LLP - - APPM/TX
3040 POST OAK BOULEVARD, SUITE 1500
HOUSTON, TX 77056

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	
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07/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,122	YAU ET AL.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-18,21-25,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-18, 21-25, 27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/23/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-18, 21, 23-25, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang ('572) in view of Matsuura (U.S. 6,124,641) and Hu et al. (U.S. 5,718,967, hereinafter Hu).

In reference to claims 15-18, 21 23-25 and 28 Chiang (Figs.15-25) teaches a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein (Chiang, column 12, lines 52 – 63); depositing a first dielectric layer (322) on said substrate (320) (Chiang, column 13, lines 15 – 35); forming an etch stop layer (323) on said first dielectric layer (322) (Chiang, column 14, line 61 – column 15, line 4); forming a second dielectric layer (350) on said etch stop layer (323) (Chiang, column 15, lines 28 – 46); forming a photoresist layer (352) on said second dielectric layer (350) (Chiang, column 15, lines 48 – 58); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350) (Chiang, column 15, lines 59 – 62), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable

spin-on polymer (Chiang, column 13, lines 15 – 35 and column 15, lines 28 – 46), and further forming a third dielectric layer (395) over said second dielectric layer (Chiang, column 21, lines 4 – 15).

Chiang fails to disclose forming the second dielectric layer using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang teach upon the claimed invention.

Chiang fails to disclose forming a low dielectric constant organosilane layer in a plasma enhanced process from a mixture comprising a methylsilane compound and an oxidizing gas, the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Matsuura (Figs.1a-1c) teaches a method of forming a dielectric stack including the steps of depositing on a substrate (1) a plurality of layers (3, 4, 5), wherein one of the layers (4) is a low dielectric constant oxidized organosilane layer comprising carbon, wherein the low dielectric constant oxidized organosilane layer (4) is deposited in a chemical vapor deposition process from a mixture comprising methylsilane or vinylsilane, and H_2O_2, and wherein the carbon content of the low dielectric constant oxidized organosilane layer is around 18% by atomic weight (See Fig.2, for example) (Matsuura, column 4, line 17 – column 5, line 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang and Matsuura to enable forming the low-k dielectric layers of Chiang according to the teachings of Matsuura because one of ordinary skill in the art at the time the invention was made

would have been motivated to look to alternative suitable methods of forming the second dielectric layer of Chiang and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because this would prevent a poisoned via from being formed in a resulting insulating film (Matsuura, column 2, lines 57 - 64).

While the combination of Chiang and Matsuura discloses a carbon content of 18% atm weight, they fail to disclose wherein the carbon content of the low dielectric constant oxidized organosilane layer is from 1% to 50% by atomic weight. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the carbon concentration in the dielectric layer of the combination of Chiang and Matsuura to arrive at the claimed invention.

The combined teachings of Chiang and Matsuura fail to expressly disclose wherein the chemical vapor deposition process is a plasma enhanced chemical vapor deposition process.

However, Hu teaches a method of forming oxidized organosilane layers including forming said oxidized organosilane layer using a plasma enhanced chemical vapor deposition process using organosilicon compounds such as a silane, siloxane or a silazane (Hu, column 3, lines 18 – 61).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chiang and Matsuura with Hu to enable the disclosed chemical vapor

deposition step of Chiang and Matsuura to be performed according to the teachings of Hu because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed chemical vapor deposition step of Chiang and Matsuura and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 27 the combined teachings of Chiang, Matsuura and Hu teach forming the low dielectric constant oxidized organosilane layer using a plasma enhanced chemical vapor deposition process disclosed in Hu et al. to U.S. 5,298,587, "...which disclosure is incorporated herein by reference..." (Hu, column 3, lines 58 – 61).

Furthermore, the provided evidence to Hu et al. (U.S. 5,298,587), discloses wherien the deposition process is performed in the presence of RF power (Hu et al., column 2, lines 30 – 48).

Therefore, the combined teachings of Chiang, Matsuura and Hu teach the claimed limitation.

3. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang ('572) in view of Matsuura ('641) and Hu ('967) as applied to claims 15-18, 21 and 23-25, 27 and 28 above, and further in view of Chen (U.S. 5,970,376).

The combination of Chiang, Matsuura and Hu substantially teach the claimed invention but fail to disclose etching the low dielectric constant oxidized organosilane layer using fluorine, carbon, and oxygen ions.

However, Chen (Figs.4-7) in a related method to form interconnect structures teaches the steps of forming a low dielectric layer (32) over a substrate (30), wherein said dielectric layer has the general formula R_1-Si$(OR_2)_3$, wherein R_1 is hydrogen and R_2 is CH_3; and etching the low dielectric layer (32) using fluorine, carbon, and oxygen ions (Chen, column 4, line 66 – column 5, line 12, column 5, lines 34 – 56, column 7, lines 25 – 42, and column 8, lines 40 – 48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang, Matsuura and Hu with Chen to enable etching the dielectric layer of Chiang, Matsuura and Hu according to the teachings of Chen for the further advantage of forming vias with attenuated lateral etching of said vias (Chen, column 4, lines 39 – 63).

Response to Arguments

4. Applicant's arguments filed 05/23/2008 have been fully considered but they are not persuasive.

Applicant argues, "…Hu does not teach deposition of an organosilicon layer from a methylsilane compound by plasma-enhanced CVD…". In response to this argument,

Hu was relied on the basis that low-dielectric layer could be formed by plasma-enhanced CVD, not on the materials used.

Applicant also argues, "...Matsuura uses plasma to deposit a silicon oxide layer from TEOS, but avoids using plasma to deposit a layer using methylsilane. Applicant thus submits that one of ordinary skill in the art, upon reading Hu and Matsuura, would be led to avoid using plasma to deposit a layer from a methylsilane compound...".

In response to this argument, Matsuura teaches depositing a low-k dielectric layer using methylsilane by a CVD process (Matsuura, column 4, lines 30 – 44). Although Matsuura is silent on which CVD process is used to form said low-k dielectric layer, Matsuura is open to different CVD such as plasma-enhanced CVD. Since the teachings of Hu provides evidence of dielectric layer formed by plasma-enhanced CVD, one of ordinary skill in the art at the time the invention was made would find obvious to use plasma-enhanced CVD for the expected result of forming the low-k dielectric layer.

It is noted that Matsuura teaches away from performing an oxygen plasma treatment on a deposited organic SOG layer (Matsuura, column 2, lines 40 – 54). However, Matsuura does not teach away from using a particular CVD process over another.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is (571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Julio J. Maldonado/
Art Unit 2823

/J. J. M./
Art Unit 2823

/Matthew S. Smith/
Supervisory Patent Examiner, Art Unit 2823